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METHOD OF AUTOMATED DESIGN AND CHECKING FOR ESD ROBUSTNESS

ABSTRACT OF THE INVENTION

A integrated circuit (IC) chip with ESD robustness and the system and method of wiring the IC chip. Minimum wire width and maximum resistance constraints are applied to each of the chip's I/O ports. These constraints are propagated to the design. Array pads are wired to I/O cells located on the chip. Unused or floating pads may be tied to a power supply or ground line, either directly or through an electrostatic discharge (ESD) protect device. A multi-supply protect device (ESDxx) coupled between pairs of supplies and ground or to return lines is also included. Thus, wiring is such that wires and vias to ESD protect devices are wide enough to provide adequate ESD protection. Robust ESD protection is afforded all chip pads. The design may then be verified.